

Curriculum Vitae

PERSONAL PARTICULARS			
Dr. KURESHI ABDUL KADIR ABDUL GANI			
Dr. Kureshi A. K. Principal M.H. SabooSiddik Polytechnic, Byculla Mumbai, Maharashtra (Aided institute of Govt. of Maharashtra) Email:principal_mhssp@rediffmail.com akkureshi@rediffmail.com		Residential Address: Dr. Kureshi A. K. Plot No. 6B Ekta Colony Govindpura Ahmednagar, Maharashtra (M.S), India -414001 Contact No.: -09970178118	
Date of Birth: 09/06/1970	Place of Birth: Ashti Dist. Beed(M.S) India	Sex:Male	Nationality: Indian Religion: Islam Marital Status: Married
Educational Qualifications: PhD (Electronics Engineering)			
Year	Institutions / University		Qualification
1994	STB College of EngineeringTuljapur B.A. Marathawada University Aurangabad, (M.S) India		B.E. (Electronics)
2004	JN College of EngineeringAurangabad B.A. Marathawada University Aurangabad, (M.S) India		M.E. (Electronics)
2010	Aligarh Muslim UniversityAligarh India		PhD(VLSI Design)
PhD Topic: “Low Power Techniques and Architecture for Field Programmable Gate Arrays (FPGAs)”			
Membership of Professional Institutions or Societies 1- Life Member of Indian Society for Technical Education (LMISTE) 2- Fellow Institution of Engineers (FIE) India 3- Member of Institute of Electrical and Electronics Engineers (IEEE) 4- Chartered Management Institution (CMI) UK			
Present Status		Name and address of employer:	
Principal		M.H. Saboo Siddik Polytechnic, Byculla Mumbai (Aided institute of Govt. of Maharashtra)	
		From 01 / 08 /2016	
Appointments			
From To	Employer (Name and address)		Position
01/08/2016 to Till date	M.H. Saboo Siddik Polytechnic, Byculla Mumbai (Aided institute of Govt. of Maharashtra)		Principal (Approved by DTE) (Aided/877 Dated 14/094/2016)
21/11/2010-31/07/2016	Vishwabharati Academy’s College of Engineering Ahmednagar, (M.S) India		Principal Approved by Pune University (CCO/3200 Dated 11/4/2011)
01/01/2009 - 20/11/2010	Padmashri Dr. VithalraoVikhePatil College of Engineering Ahmednagar, (M.S) India		Professor Approved by Pune University

		(CCO/1613 Dated 01/02/2011)
01/07/2004 - 31/12/2008	Padmashri Dr. VithalraoVikhePatil College of Engineering Ahmednagar, (M.S) India	Assistant Professor Approved by Pune University (CCO/3994 Dated 07/06/2005)
29/7/1998 - 30/6/2004	Padmashri Dr. VithalraoVikhePatil College of Engineering Ahmednagar, (M.S) India	Lecturer Approved by Pune University (CCO/36 Dated 27/11/1999)
01/6/1995 - 15/7/1998	Amrutvahini College of EngineeringSangamner, (M.S) India	Lecturer
Total experience ~ 25 years		
Specialization:- Nano-devices, CNFET/CNT Interconnect, FPGAs, Hspice, VHDL and Verilog.		
Subject Taught:- VLSI Design,Nano-electronics,Digital Design, Analog Electronics, Power Electronics, Optical Fiber Communication, Electronics Instrumentation & Measurement, Mechatronics, Bio-Medical Electronics and ResearchMethodology.		
PUBLICATIONS		
A. Refereed Journals		
1- Kureshi A. K. and Mohd. Hasan, “Performance comparison of CNFET and CMOS based 6T SRAM cell in deep submicron,” Microelectronic Journal, Vol.40, No.6, pp.979-982, June-2009.		
2- Kureshi A. K. and Mohd. Hasan, “Analysis of CNT bundle and its comparison with copper interconnect for CMOS and CNFET drivers,” Journal of Nanomaterials, pp. 1-6, 2009.		
3- Kureshi A. K. and Mohd. Hasan, “DTMOS based low power high speed interconnects for FPGA,” Journal of Computers, Vol.4, No.10, pp.921-926, Oct-2009.		
4- Kureshi A. K. and Mohd. Hasan, “Analysis of CNT bundle and its comparison with copper for FPGAs interconnects,” International Journal of Applied Science, Engineering and Technology, Volume 5:3, pp.178-183, 2009.		
5- Kureshi A. K. and Mohd. Hasan, “Leakage analysis and optimization of CLB in Vertex-II FPGAs,” International Journal of Systemic Cybernetic and Informatics, Vol.3, No.1, pp.2718-2722, Nov-2007.		
6- Kureshi A. K. and Mohd. Hasan, “DTMOS based low power FPGAs building blocks,” Mediterranean journal of Electronics and Communication, Vol.6, No.4, pp.120-125, Oct-2010.		
7- S.D. Pable, Mohd. AjamalKafeel, A. K. Kureshi and Mohd. Hasan, “Robustness Comparison of Emerging Devices for Portable Application,” Journal of Nanomaterials, pp. 1-8, 2012.		
8- Kureshi A. K. and Mohd. Hasan, “Performance Optimization and Comparison of CNT Interconnect with Copper at VDSM Technology,” International Journal of Management & Information Technology, Vol.6, No.2, pp.826-834, Oct-2013		
9- KunalSubhashKhandelwal and Kureshi A. K. “Robust Design Challenges in Low NoiseAmplifier,” International Journal of Innovative Research in Science, Engineering and Technology, Vol.3, No.4, pp.343-349, April-2014.		
10- Madge Deepali Harish, Bhojraj R. Patil and Kureshi A. K. “Design of Sub Threshold Flip Flop For UltraLow Power Applications,” International Journal of Innovative Research in Science, Engineering and Technology, Vol.3, No.4, pp.319-324, April-2014.		

- 11- Madge Deepali Harish and Kureshi A. K. "Design of Pulse Triggered FlipFlop for Low Power Applications," International Journal of Electronics Communication and Computer Technology, Vol.5, No.1, pp.795-798, Jan-2015.
- 12- Navendu Kumar, Dr. A K Kureshi, Mr. Prerak Vyas "Control System Design and Development of DSP based Controller for Servo Payload System," International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Vol.4, No.7, pp.1895-1900, July-2015
- 13- Kunal Subhash Khandelwal and Kureshi A. K. "A 2~8 GHz UWB Low Noise Amplifier using 0.15 μ m GaAs pHEMT Technology for Multiband Wireless Application," Journal of Communications on Applied Electronics, Vol.3, No.3, pp.1-5, Oct-2015.
- 14- S. B. Rahane and A K Kureshi, "A Low Power and Linear Voltage Controlled Oscillator Using Hybrid CMOS- CNFET Technology," International Journal of Applied Engineering Research, Vol.12, No.9, pp.1069-1073,
- 15- S. M. Turkane, G. K. Kharate and A. K. Kureshi, "Ge/Si Hetero-Junction Hetero-Gate PNPn TFET with Hetero-Dielectric BOX to Improve ION/IOFF," Indian Journal of Science and Technology, Vol.10, No.14, pp.1-7.
- 16- S. M. Turkane, G. K. Kharate and A. K. Kureshi, "Emerging interconnects: a state-of-the-art review and emerging solutions," International Journal of Electronics, Vol 104, No.7, pp.1107-1119.

B. Refereed International Conferences

- 17- Abdul Kadir Kureshi, Mohd. Hasan, and Naushad Alam, "Subthreshold deep submicron performance investigation of CMOS and DTCMOS Biasing Schemes for Reconfigurable Computing," IEEE ISCAS, Taiwan, pp. 2545-2548, May 2009.
- 18- Mohd. Hasan and Abdul Kadir Kureshi, "Leakage reduction in FPGA routing multiplexers," IEEE ISCAS, Taiwan, pp.1129-1132, May 2009.
- 19- Naushad Alam, A. K. Kureshi, and Mohd. Hasan, "Carbon nanotube interconnects for low-power high-speed applications," IEEE ISCAS, Taiwan pp.2273-2276, May 2009.
- 20- A. K. Kureshi and Mohd. Hasan, "Energy efficient high speed CNFET based interconnect drivers for FPGAs," International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT-09) pp.48-51, March 2009.
- 21- Naushad Alam, A. K. Kureshi, and Mohd. Hasan, "Analysis of carbon nanotube interconnects and their comparison with Cu interconnects," International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT-09), pp.124-127, March 2009.
- 22- Naushad Alam, A. K. Kureshi, and Mohd. Hasan, "Performance comparison and variability analysis of CNT bundle and Cu interconnects," International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT-09), pp.169-172, March 2009.
- 23- Kureshi A. K., Naushad Alam, and Mohd. Hasan, "A novel low power high speed field programmable gate array routing interconnect," in the proceedings of SPIT-IEEE Colloquium and International Conference, Vol. 2, pp. 145 – 149, Feb. 2008.
- 24- Naushad Alam, Kureshi A. K., and Mohd. Hasan, "Analysis and comparison of subthreshold 1-bit full adder cells", in the proceedings of SPIT-IEEE Colloquium and International Conference, Vol. 2, pp. 127 – 131, Feb. 2008.

- 25- Kureshi A. K. and Mohd. Hasan, "Leakage power estimation and minimization in CLB of FPGA," Proceedings of the IEEE-International Conference on Computer and Communication Engineering, Kuala Lumpur, Malaysia, pp.270-274, May 13-15, 2008.
- 26- Tarun Kumar Agarwal, AnuragSawhney, Kureshi A. K. and Mohd. Hasan, "Performance comparison of static CMOS and MCML gates in sub-threshold region of operation for 32nm CMOS technology," Proceedings of the IEEE-International Conference on Computer and Communication Engineering, Kuala Lumpur, Malaysia, pp.284-287, May 13-15, 2008.
- 27- Kureshi A. K. and Mohd. Hasan, "Low power field programmable gate array interconnects," in the proceedings of the 5th International Conference on Systemics, Cybernatics and Informatics(ICSCI 2008), Vol. 1, pp. 52 – 55.
- 28- *NaushadAlam, Kureshi A. K., and Mohd. Hasan, "Subthreshold CMOS full adder for ultra-low power operation," in the proceedings of the 5th International Conference on Systemics, Cybernatics and Informatics(ICSCI 2008), Vol. 1, pp. 48 – 51
- 29- Kureshi A. K. and Mohd. Hasan, "Leakage analysis of CNFET based basic digital building blocks," in the proceedings of International Conference on Embedded System and VLSI Design (ICEVD 2008), pp. 246 – 249
- 30- Kureshi A. K. and Mohd. Hasan, "Leakage power and delay optimization of FPGA interconnects," IEEE-International Conference on Signal processing, Communications and Networking (ICSCN 2008), pp.568-572, Jan 2008.
- 31- Kureshi A. K. and Mohd. Hasan, "Low leakage high speed CNFET based look up table," IEEE-International Conference on Emerging Trends in Electronics Technology), pp.432-436, July 2008.
- 32- Fahadaliusmani, A. K. Kureshi, Mohd. Hasan, and M.J.R. Khan, "Performance analysis of bulk CMOS, strained silicon and CNFET based operational amplifiers in VDSM technology," IEEE International Advance Computing Conference (IACC), pp. 2567-2579, March- 2009.
- 33- A.U. Kadu, Prof. S. M. Turkane, Dr. S. D. Pable and Dr. A. K. Kureshi, "Implementation of a Novel Co-Design of LVTSCR for Effective ESD Protection in Ultra-deep Submicron IC," International Conference on Industrial Instrumentation and Control (ICIC), Pune, India, pp.39-42, May 2015.
- 34- S. M. Turkane and Kureshi A. K., "Analysis of Double Gate Tunneling FET characteristics for low power designs Suppression," 2nd International conference on Innovative Engineering Technologies (ICIET-2015), Bangkok, Thailand, pp.10-14, August 2015.
- 35- RahaneSandip, Kureshi A. K. and Pable S. D., "A Hybrid CMOS-CNFET, 1.4-V 6.8-ppm/°C Bandgap Reference Circuit," 12th IEEE Int. Conference (INDICON-2015), New Dehli, India, pp.110-114, Dec 2015.

C. National Conferences

- 36- Kureshi A. K., and Mohd. Hasan, "Performance comparison of CNFET and CMOS based 8T SRAM Cell in deep submicron," 12th IEEE VLSI Design and Test Symposium (VDAT-08), pp.270-274, July 2008.
- 37- NaushadAlam, Kureshi A. K., and Mohd. Hasan, "Dynamic threshold PMOS switch for power gating," 12th IEEE VLSI Design and Test Symposium (VDAT-08), pp.317-320, July 2008.
- 38- Anurag Agarwal, Kureshi A. K., and Mohd. Hasan, "Dynamic threshold PMOS switch for power gating," 12th IEEE VLSI Design and Test Symposium (VDAT-08), pp.426-430.
- 39- Kureshi A. K. and Mohd. Hasan, "Subthreshold operation of field programmable gate array," In the

proceedings of MTECS, pp. 244 – 247, March 2008.

40- Kureshi A. K. and Mohd. Hasan, “Interconnect performance comparison of FPGA at 32nm technology,” in the proceedings of NSC-08 (IIT Roorkee), pp. 766 – 769, 2008.

41- Kureshi A. K. and Mohd. Hasan, “Leakage analysis and optimization of SRAM cell at 32nm,” in the proceedings of NSC-07, pp. 123 – 126, 2007.

39- Kureshi A. K. and Mohd. Hasan, “A study of different circuit level techniques for low leakage SRAM cells,” In the proceedings of NCACCN, pp. 438 – 411, Feb 2007.

D. Publication of Books

Published a book on ‘**COMMUNICATION ENGINEERING**’ By Everest Publication.

List of ISTE/QIP/Short term courses attended: (ISTE: Indian Society for Technical Education, QIP: Quality Improvement Programme)

Institute	Title	Duration
Government COE, Pune	A course on “VLSI Design” under the project IMPACT ministry of IT government of India.	15/6/2001-10/7/2001 ~ 4 Weeks
SKNCOE, Pune	Advance VLSI Design	16/6/2002-30/6/2002 2 Weeks
Dr. BATU, Loneri	Biomedical Signal and Image Processing	10-21 March-2003 2 Weeks
I.I.T. Mumbai	FPGAs Design under Xilinx University Program	30/9/2003-1/10/2003
VJTI Mumbai	Renewable Energy sources, material and policies	27/12/2014-02/01/2015
VJTI Mumbai	Recent Trends in Power Electronics, Drives and Storage Technology for Emerging Application	05-09 Oct-2015
I.I.T. Bombay	INUP Familiarization workshop on Nanofabrication Technology	16 to 18 Dec-2015
I.I.T. Bombay	Hands-on Training Workshop on Nanofabrication Technologies	18 to 22 Jan-2016
UKIERI	Leadership Development Program Organized by Govt. of UK in collaboration with Govt. of India.	4-Week 28 th -30 th June-2017, 31 st July-2 nd August-2017, 3 rd -6 th Oct-2017, 10 th -12 th Jan-2018

Awards Received

- 1- *Best paper award at International Conference by Pentagonam research center Hyderabad
- 2- Engineering Achievement award by Institution of Engineers Ahmednagar local center.

Recognized as PhD guide at Following University

- 1- Pune University for Electronics and Telecommunication Engineering
- 2- Dr. BAM University Aurangabad.

Presently four research scholars have completed and four are pursuing their PhD under my guidance at S P Pune University and Dr. BAM University, Maharashtra

- Robust Ultra Low Power Operational Amplifier Design in very Deep Submicron Technology.
Name of Research Scholer :- BendreVarshaSachin, completed on 2nd August 2020
- Design of Energy Efficient Field Programmable Gate Arrays for Moderate Speed Applications.
Name of Research Scholer :- SatishMohanraoTurkane, completed on 22nd April 2018
- Design of Ultra Low Power Circuits Using Nano-scale Hybrid Technology.

Name of Research Scholer :- Sandip Bhagwat Rahane, completed on 18th April 2019

- Real Time ECG Transmission via Wireless Commuincation.

Name of Research Scholer :- Devendra Laximan Bhuyar, completed on 18th March 2021

Research Experience

Guided ~ 70 under-graduate projects.

Guided 20 Post-graduate projects few of them are as:

- 1) Realization of Micro-Strip Band Pass Filter Design
- 2) Robust Design of Sub Threshold Sequential CMOS Elements for Low Power Application
- 3) Analysis of Different Stenographic Techniques on FPGA
- 4) Control System Design & Development of DSP Based Servo Pay Load System
- 5) VLIW Processor Implementation on FPGA & Its Application
- 6) Hardware Implementation of Booth multiplier on FPGA
- 7) Real Time Bluetooth Communication between FPGA & Android Phone
- 8) UVM Rapid Adoption: A Practical Subset of UVM

Worked as Resource Faculty and handled other portfolios are as:

- Delivered a Invited talk at AICTE sponsored SDP (Staff Development Program) on Carbon Nanotube in VLSI Design at Amrutvahini College of Engineering Sangamner on 01st Oct-2009.
- Delivered a lecture in CUP (Content Updating Program) on VLSI Design at Amrutvahini Polytechnic Sangamner on 5th Jan-2011.
- Delivered a lecture in CUP on VLSI Design at K KWagh Polytechnic Nashik on 8th Feb-2012.
- Delivered a lecture in CUP on VLSI Technology at Samarth Polytechnic Belhe on 31st Dec-2012.
- Delivered a lecture in CUP on 3D VLSI and Embedded Technology at Government Polytechnic, Ahmednagar 4th Jan-2013.
- Adjunct Faculty for M.E. (Embedded and VLSI Design) at PC College of Engineering Pune.
- Worked as Chairmen of VLSI Design subject of final year UG course of Engineering of Pune University.
- Worked as Examiner of VLSI Design subject of final year UG course of Engineering of Pune University.
- Acted as chairmen of dissertation committee of M.E. (Embedded and VLSI Design) at present institution.
- Worked as Senior Supervisor for Theory Examination of the center at Pune University.
- Participated as an Expert in the revision of syllabus of VLSI Design subject of final year UG course of Engineering of Pune University.
- Worked as Assistant warden in Amrutvahini College of Engineering Sangamner.
- Worked as Chief warden in Amrutvahini College of Engineering Sangamner
- Worked as Assistant warden in Padmashri Dr. VithalraoVikhePatil College of Engineering Ahmednagar
- Invited as Session chair in National and International conference held at various institutes.
- Invited as Examiner for the conduction of Dissertation of M.Tech students of other Universities in the state of Maharashtra.